Dean&Francis
ISSN 2959-6157

Research on System-level Design Challenges and Solutions for 3D Chiplet Integration

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Abstract:

With the slowdown of Moore's Law and the exponential increase in the cost of advanced manufacturing processes, heterogeneous integration technology based on chiplets has become the key path for the continuation of the development of the integrated circuit industry. This technology achieves an optimal balance of system performance, cost and flexibility by densely stacking chip wafers of different process nodes and functions in a three-dimensional space. However, from the perspective of system-level design, three-dimensional chiplet integration brings unprecedented challenges in aspects such as architecture partitioning, interconnection standards, physical integration, and design methodologies. This article systematically reviews the core challenges in the design process of three-dimensional chiplet systems, discusses the solutions from system architecture exploration to physical implementation, and looks forward to the future design automation tools and collaborative optimization methods for the chiplet ecosystem.

Keywords: Chiplet; Heterogeneous Integration; Three-Dimensional Integration; System-level Design; Advanced Packaging; Design Methodology

1. Introduction

In the post-Moore era, the path of simply relying on reducing the feature size of transistors to enhance chip performance has gradually reached its physical limit. The costs for advanced process nodes, such as 5nm and below, for wafer fabrication are as high as several hundred million dollars. Due to the increase in defect density as the area expands, resulting in a decline in yield; due to the escalation in complexity, leading to excessively long design and verification cycles; and due to the lack of flexibility when optimizing functions for different processes in combination or reusing intellectual property across multiple products [1].In this context, the core-shield technology emerged. Its essence is to divide a complete on-chip system into multiple independent "cores" based on functional modules, manufacture each of them using the most suitable process node, and then achieve high-density interconnection and integration

on the same substrate through advanced packaging technology [2].This approach of breaking things down into smaller parts brings about numerous advantages. Different functional modules can adopt the most suitable process nodes for calculation, aiming to achieve high performance by using the most advanced manufacturing processes. Meanwhile, I/O, analog circuits, etc. use mature processes to control costs [3].The yield rate of single units of small-sized chips is much higher than that of large-sized single chips, which helps to reduce manufacturing costs [4].Moreover, the chiplet technology enables the hard-core reuse of IP. The design team can assemble chiplets from different suppliers like building blocks, significantly shortening the product development cycle and enhancing design flexibility. The emergence of three-dimensional chiplet integration has fundamentally changed the system-level design paradigm of chips. The traditional chip design was a top-down, closed process based on a single chip, where all modules had to be completed under the same process platform and by the same design team. The core module design has shifted towards an open ecosystem of multi-source heterogeneity and collaborative design. Different core modules may be designed by different manufacturers, manufactured using different processes, and follow different interface protocols. Eventually, they are integrated into a single unit through advanced packaging. This transformation has introduced new complexities to various aspects such as system architecture division, inter-core interconnection communication, physical integration, and cross-level design verification [5].This article aims to take a system-level perspective and systematically explore the core design challenges of three-dimensional chiplet integration. It discusses these challenges from various dimensions such as system architecture partitioning, interconnection and interface circuit design, physical integration, design methodologies and EDA tool chains, testing and yield. It also reviews the representative solutions adopted by the academic and industrial communities to address these challenges, and looks forward to the future directions of design automation and collaborative optimization for the chiplet ecosystem.

2. Core Design Challenges of Three-Dimensional Chip System Integration

Three-dimensional chip-scale integration shifts the system design from the traditional single-chip closed process to a multi-source heterogeneous open ecosystem. This transformation has triggered new complexities at multiple levels, including system architecture partitioning, interconnection and interface circuits, physical integration, and design methodologies. First, at the level of system architecture division, the functional modules that were originally completed within a single chip have now been divided into multiple independent cores. How to reasonably define the functional boundaries among different process nodes and different suppliers becomes a key factor determining the system's performance, power consumption, and cost. Unlike traditional system-on-chip architectures where each module can achieve close coupling through sharing the same process library and unified design process, in a core-merging system, the interconnection bandwidth, packaging costs, and compatibility with heterogeneous processes must be considered during the early architecture exploration stage. This imposes higher requirements on the scale of the design space and the complexity of decision-making [6].The inter-chip interconnection communication lacks unified, open and widely compatible interface standards. Although some candidate solutions such as UCIe and BoW have emerged in the industrial field, practical integration still faces real problems such as protocol adaptation, electrical mismatch and physical layer compatibility [7].The widely adopted interconnection structures such as silicon vias and micro bumps in three-dimensional stacking further introduce challenges such as signal integrity, thermal stress coupling and power integrity. The interface circuit must achieve extremely high bandwidth density within a limited area and power budget, significantly increasing the design difficulty [8].At the level of physical integration and design, issues such as thermal management, mechanical stress, and power supply network design in three-dimensional stacking exhibit nonlinear coupling characteristics, and traditional two-dimensional design processes are difficult to be directly extended. When multiple cores are stacked vertically, the power density increases sharply, and the distribution of hotspots and the heat dissipation path become complex. Moreover, the thermal field and stress field will interact with each other, causing changes in timing, reliability, and even the physical structure [9].The current electronic design automation toolchain still focuses on a single chip, lacking effective support for multi-source heterogeneous chiplet co-design and cross-level simulation and joint verification. Design teams need to manually transfer data between multiple tool platforms, resulting in long design convergence cycles and high iteration costs. Testing and yield issues are more prominent in three-dimensional integration. Even if each die is a known good product before packaging, the overall yield may still decrease due to interconnection defects, thermal stress failure, or abnormal power supply networks after integration [10].The testability design for three-dimensional packaging is not yet mature. The fault isolation and diagnosis mechanisms are

ISSN 2959-6157

difficult to cover the deep fault points in the stacked structure. This makes the test strategy for three-dimensional chiplet systems have to shift from single-chiplet testing to packaging-level collaborative testing, and introduce new mechanisms such as hierarchical testing and adaptive repair [11].

3. System-level solutions and key technologies for three-dimensional chip integration

3.1 Architectural innovation and open interconnection standards

The academic community and the industrial sector have proposed system-level solutions from multiple perspectives including architectural innovation, interconnection standards, physical collaborative design, and design automation. At the architectural level, the adoption of open interconnection standards has become a key driving force for reducing the barriers to heterogeneous chip integration. The current mainstream core interconnection standards have different focuses in terms of physical layer implementation, protocol support, and application positioning. UCIe is based on the PCIe/CXL protocol system, supporting standard packaging and advanced packaging, and has a complete ecosystem foundation, suitable for scenarios such as high-performance computing and data centers [12]; BoW focuses on low-cost and low-latency short-distance interconnection, and performs outstandingly in terms of power efficiency [13]; while OpenHBI is oriented towards high-bandwidth memory integration, emphasizing high-density and high-energy-efficiency parallel interconnection [14].The common goal of these standards is to achieve plug-and-play integration of chips from different manufacturers within the same package by clearly defining the interface specifications between the physical layer and the protocol layer. The role of system-level architecture exploration tools becomes increasingly prominent during the early design stage. Design teams can quickly evaluate different partitioning schemes, interconnection topologies, and packaging options to find the optimal balance between power consumption, performance, and cost. The multi-vendor collaborative design framework has also gradually taken shape. By clearly defining interface specifications, design boundaries, and responsibility divisions, it further shortens the product development cycle.

Table 1. Comparison of mainstream interconnect standards

Standard	Physical layer implementation	Protocol support	Main application scenarios
UCIe	Advanced packaging / Standard packaging	PCIe, CXL, streaming protocol	High-performance computing, data centers, general chip integration
BoW	Silicon interlayer, silicon bridge	Customized parallel protocol	Low latency and high energy efficiency close-range interconnection
OpenHBI	Silicon interlayer	HBM-like protocol	High-bandwidth memory integration, storage-class die

3.2 Technological Evolution and Future Trends

Looking ahead, the three-dimensional chiplet integration technology will continue to evolve along the directions of standardization, intelligence and system-level collaboration. System-level collaborative design will become the core competitiveness. The boundaries between chip design, packaging manufacturing and system verification will become increasingly blurred. The design team needs to complete the joint optimization from transistors to the system within a unified data model and collaborative framework. With the continuous maturation of open standards, collaborative design frameworks, and multi-physics field optimization tools, three-dimensional chiplet integration will gradually shift from the current customized solutions to a platform-based and automated design paradigm, laying a solid foundation for the innovation of integrated circuits in the post-Moore's era.

4.Conclusion

Three-dimensional chip-scale integration technology, as an important path for the continuation of integrated circuit industry development in the post-Moore era, achieves the coordinated optimization of system performance, cost and flexibility through heterogeneous integration and advanced packaging. However, this technological paradigm, from the perspective of system-level design, has brought about profound challenges in multiple dimensions such as architecture division, interconnection standards, physical integration, and design methodologies. This article systematically reviews the core design challenges of three-dimensional chiplet system integration, and points out that key issues such as function boundary division,

compatibility of interconnection interfaces, multi-physical field coupling of heat, force and electricity, and insufficient support from EDA toolchains are currently restricting the large-scale development of the chiplet ecosystem. In response to the aforementioned challenges, this article further reviews the representative solutions in the fields of architecture innovation, interconnection standards, collaborative design, and test yield rate that have been proposed by the academic community and the industrial sector. From the current development trend, three-dimensional chiplet integration is evolving from customized and fragmented solutions to platform-based and automated design paradigms. System-level collaborative design will become the core competitiveness, and the boundaries between chip design, packaging manufacturing, and system verification will further merge. Overall, three-dimensional chiplet integration demonstrates great potential in addressing the performance and cost challenges of the post-Moore era. However, its system-level design methodology still needs to be further developed in aspects such as the unification of open standards, the improvement of collaborative design frameworks, and the breakthroughs in multi-physics field optimization tools. In the future, as the chiplet ecosystem continues to mature and the level of design automation improves, three-dimensional chiplet integration technology will provide a solid foundation for the efficient innovation of the integrated circuit industry.

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